REMARKS

Claims 1-32 remain pending in the application. Claims 1 - 3, 5, 6, 8 - 12, 14, 17 - 19, 21, 23 - 26, and 28 -30 have been amended.

Objections to the Drawings:

The drawings were objected to. In a first objection, the Examiner states that the LSSD clocks and STEP clocks shown in Figure 2 are not referred to in the disclosure. Applicant respectfully disagrees, and submits that both the LSSD clocks (also shown as LSSD_CLKA and LSSD_CLKB in Figure 9) and the STEP clocks (shown in Figure 9 as the clock signals of LBST_STEP_CLKC and LBST_STEP_CLKE) are referred to in the paragraph beginning on page 9, line 29, in conjunction with Figure 9.

The drawings were also objected to because the LSSD_CLKA, LSSD_CLKB, LBST_SCAN_CLKA and LBST_SCAN_CLKB were not referred to in the disclosure. Applicant has amended the disclosure to include reference to the LSSD_CLKA and LSSD_CLKB signals, which are the LSSD clocks discussed above. Applicant has amended Figure 9 to remove the LBST_SCAN_CLKA and LBST_SCAN_CLKB references.

Objection to the Specification:

The specification was objected to for various informalities. Applicant has amended the specification to correct these informalities.

Objections to the Claims:

Claims 1, 2, 8, 10, 11, and 18 were objected to for informalities. Applicant submits that the amended version of each of these claims meets formal requirement, and thus respectfully requests removal of the claim objections.

35 U.S.C. § 112 Rejections:

Claims 5, 14, 19, 21, 23, 24, 25, 26, 28, and 29 were rejected under 35 U.S.C. § 112 for insufficient antecedent basis for various claim limitations. Applicant submits that there is sufficient antecedent basis for all limitations recited in the amended versions of these claims, and respectfully requests removal of the § 112 rejections.

35 U.S.C. § 103 Rejections:

Claims 1, 2, 6-10, 15, 17 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Motika, U.S. Patent 5,982,189, in view of Rosno, U.S. Patent 6,535986. Claims 21 and 25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rosno in view of Kraus, U.S. Patent 6,587,979. Claims 26, 31, and 32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Au, U.S. Patent 6,681,359 in view of Zuraski, U.S. Patent 6,560740, Motika and Rosno. Applicant respectfully traverses these rejections.

The cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims. Motika teaches a built-in stress circuit for an integrated circuit that has a frequency generator, at least one self-test circuit, a temperature regulator and a controller. The frequency generator receives a reference clock and an adjusted temperature frequency from the temperature regulator and outputs the test frequencies needed for the self-test circuits. The self-test circuits, which are coupled to the frequency generator, receive the test frequencies and dissipate power as the self-test circuits are being used. The temperature regulator, which is coupled to the self-test circuits and the frequency generator, senses the power dissipated (i.e., the temperature), adjusts a temperature frequency corresponding to the temperature desired, and outputs the adjusted temperature frequency. The controller, which is coupled to the frequency generator, the self-test circuits, and the temperature regulator, provides the control data necessary for testing both electrical and thermal stress conditions.

Rosno teaches a method of adjusting the operating or timing margin of a clocked system, such as a digital computer or a memory controller, is disclosed. The method may

be automated to occur upon every initial program load or can be manually adjusted for changes in frequency, operating voltages, or applications in which the timing margin is not so critical. An initial or default frequency of the clock is set. Clock control settings, such as duty cycle, VCO range and gain, etc, are also initialized and set as some default. Test, such as ABIST, LBIST or other functional tests, are performed on the clocked system and the clock frequency is incrementally increased until the tests fail. Upon failure of the tests, one or more clock control settings are adjusted and the tests are run again at the failing frequency. If the tests successfully complete, indicating no errors, the clock frequency is incremented again until the test fail. Again, the clock control settings are adjusted and the tests are repeated at increasing frequency until failure of the tests or until a desired timing margin is reached.

Au teaches a circuit, method and test architecture may be used for testing one or more integrated circuits that may be arranged upon a printed circuit board. Along with internal logic used by the integrated circuit during normal functioning, circuitry is included for built-in self-test. In an embodiment, the integrated circuits are semiconductor memories and include Memory Built-In Self-Test (MBIST) capability. A JTAG-compliant interface may be used to control the MBIST circuitry so that MBIST test modes can be selected by the JTAG Test Access Port controller, and MBIST test results can be written into boundary scan cells and scanned out through the JTAG Test Data Out port. The addition of a high-speed clock signal to the standard 4-wire JTAG interface allows full-speed operation of the MBIST circuitry. Therefore, the integrated circuit can be tested at full speed, and the test results scanned out by the slower JTAG clock. The use of the JTAG interface with MBIST allows multiple interconnected devices to be tested using a single interface. This is advantageous for in-circuit testing, since it is not necessary to directly probe each device to be tested. It also simplifies the use of automated test equipment, since the JTAG standard is widely used.

In contrast, independent claim 1 recites:

"A built-in self-test controller, comprising a logic built-in self-test domain configured to perform a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test." (Emphasis added).

Independent claims 7, 10, 17, 21, and 26 recite similar combinations of features.

None of the cited references, either taken singly or in combination with each other, teach or suggest the combinations of features recited in the independent claims. In particular, Applicant can find no teaching or suggestion of performing a built-in self-test at a frequency at least a slow as the slowest frequency of a plurality of timing domains to undergo the built-in self-test. In the Office Action, the Examiner states that Rosno teaches this feature in column 1, lines 64-67, column 2, lines 1-12, column 3 lines 66-67 and column 4, lines 1-10. Applicant respectfully disagrees with the Examiner's assertion, and notes that none of these citations refer to a plurality of timing domains. Applicant further notes that these citations merely refer to leaving a sufficient timing margin in the clock frequency of a circuit to prevent the circuit from failing. However, Applicant can find no teaching or suggestion in Rosno to modify Motika (as applied to claims 1, 7, 10, and 17), or Au (as applied to claim 26) in order to obtain a combination including the performing of a self-test at a frequency at least as slow as a slowest frequency of a plurality of timing domains. Applicant further submits that the combination of Rosno and Kraus, as applied to claim 21 (which also recites performing a built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains) does not teach or suggest the combination of features recited in that claim for at least these reasons. Accordingly, Applicant submits that the standard for obviousness has not been met and therefore respectfully requests removal of the 35 U.S.C. § 103(a) rejections.

With respect to the remaining § 103(a) rejections, Applicant notes that the claims subject to these rejections are dependent upon various ones of the independent claims discussed above, and thus are believed allowable for at least the same reasons.

CONCLUSION

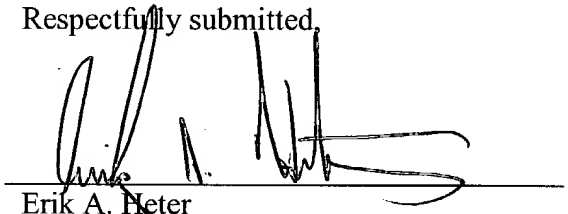
Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-56300/BNK.

Also enclosed herewith are the following items:

☐ Return Receipt Postcard

Respectfully submitted,



Erik A. Heter
Reg. No. 50,652
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: August 11, 2004